being drawn to a non-elected invention. Claim 69 has been added. There is no change as to inventorship based on provisional election and the proposed claims to a non-elected invention.

Claims 1-4, 13, 14, 16, 21, 57, and 69 are pending in the present patent application. The examiner has rejected claims 1-4, 13, 14,16, 21, and 57. Applicant respectfully requests reconsideration of claims 1-4, 13, 14,16, 21, 57 and new claim 69. in the view of at least following remarks.

I Objection to Figure 11:

The Examiner has objected to Figure 11 for failing to label the element according to its function. The Examiner has rejected the Figure 11 as follows:

> "Element 1500 in Fig. 11 should be labeled as --RF Switch-- as described in the specification."

Please make the corrections as shown in red on the attached drawing for Figure 11.

II Objection to Claim 15:

The Examiner has objected claim 15 citing that at line 1, "3" should be changed to --13--. The Examiner has objected claim 15 as follows:

> "Based on the limitation "the electrical output" in the claim, which refers to "the electrical output" recited in claim 13. Since there is no "electrical output" recited in the base claim 3. Appropriate correction is required"

Applicant has cancelled claim 15 as drawn to a nonelected invention.

III Rejection of Claim 3-12 Based on 35 U.S.C § 112, second paragraph:

The Examiner has objected claims 3-12 under 35 U.S.C. § 112 as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The Examiner has rejected the claims 3-12 as follows:

"Claim 3 recites the limitation "said isolator means" on line 1 lacks clear antecedent basis. It is unclear if this isolator means is the same as the "isolator" recited in claim 1 (or a different "isolator"). From the specification and drawings, it appears that "said isolator means" should be changed to --said isolator--. Claims 4-12 render indefinite by the deficiencies of base claim 3."

Applicant submits amended claim 3. Claims 5 – 12 have been cancelled.

IV Rejection of Claim 1-4,13,14,16,21 and 57 Based on 35 U.S.C § 102(b) as being anticipated by Barta et al.(U.S. Patent No. 4,975,604):

The Examiner has rejected the independent claims 1 and 13 based on 35 U.S.C § 102(b) as being anticipated by Barta et al.(U.S. Patent No. 4,975,604).

The Examiner has rejected the independent claim 1 as follows:

"With regard to claim 1, Barta et al discloses in Fig. 2 an electronic isolator between as source stage(22) and a load stage(24), including configuring means(12,14) for configuring the isolator (30,32,34,36) to appear as an infinite impedance to the source stage (when 34 is off, and 30 is on)."

The Examiner has rejected the independent claim 13 as follows:

"With regard to claim 13, the reference disclosed in Fig. 2 an electronic isolator between a source electrical connection connected to the source stage(inherent), an electrical output(24) comprising at least one load electrical connection to the load stage, at least one circuit path(30-34) into which electrical noise is directed away from the source and load electrical connections."

Applicant respectfully disagrees and submits that independent claims 1 and 13 are in a condition for allowance and argues as follows:

Independent claims 1 and 13 include the following limitation,

"...an electronic isolator including at least one circuit path at all into which electrical noise is directed away from said source and said load stages..."

Barta et al. does not teach, suggest or describe an electronic isolator including at least one circuit path into which electrical noise is directed away from said source and said load stages

The Examiner states that Barta et al. clearly teaches configuring the isolator (30,32,34,36) to appear as an infinite impedance to the source stage when 34 is off, and 30 is on. For example, The Examiner in the Office action dated 3/15/2002 at page 4 line 10 to page 5 line 1 states as follows:

> "Barta et al discloses in Fig. 2 an electronic isolator between as source stage(22) and a load stage(24), including configuring means(12,14) for configuring the isolator (30,32,34,36) to appear as an infinite impedance to the source stage (when 34 is off, and 30 is on)."

Hence in Barta et al., when 34 is Off there is not even one circuit path into which electrical noise is directed away from said source and said load stages. Therefore, Barta et al. does not teach, suggest or describe an electronic isolator including at least one circuit path into which electrical noise is directed away from said source and said load stages.

Moreover, the present invention is an electronic isolator, not an attenuator, that is placed between the output of one electronic circuit (source stage) and the input of a second electronic circuit (the load stage). An electronic isolator provides highly asymmetric/non-reciprocal attenuation of the electrical signal passing between source stage and load stage (See Summary of present patent application, first paragraph). An electronic isolator is defined as a device that permits a signal to pass in one direction while providing high isolation to energy in the reverse direction. In contrast, Barta et al clearly states use of attenuators and does not teach, suggest or describe an electronic isolator. The invention of Barta et al does not even mention the word "isolator". The invention of Barta et al is clearly an attenuator, as indicated by its title, not an isolator. An attenuator is defined as a circuit that reduces the power level of a signal by a certain amount (gain), with little or no reflections. Unlike isolators, attenuators have symmetric characteristics. Barta et al at column 4 lines 22-57 states as follows:

> "In accordance with a preferred embodiment of the invention, FIG. 2 shows the combination of a bridged-T attenuator cell 10 and a reference attenuator cell 12 and an operational amplifier 14. (Input protection and level shifting circuits on the control input are not shown.). This circuit is arranged to maintain, for example, a 50-ohm impedance

for RF input and output signals by adjusting the shunt FET gate voltage in the attenuator cell in response to an arbitrary voltage variation on the series FET gate.

The circuit has an attenuation control signal input 16. This input is coupled to the attenuator cell, through a resistor 18, to the gate of a series FET 20. The series FET has a source and drain symmetrically coupled to RF input/output terminals 22, 24 through series capacitors 26, 28. These capacitors are used for dc blocking so that the circuit can operate from a single power supply with appropriate level shifting (not shown) They can be omitted to extend bandwidth to lower frequencies. A pair of 50-ohm resistors 30, 32 are connected from the source and drain, respectively, of series FET 20 to the drain of a shunt FET 34. The source of the shunt FET is connected to ground or other suitable reference voltage (referred to as "ground" hereinafter). Referring back to FIG. 1B, the attenuator cell 10 as so far described has the same input and output characteristic impedances--50 ohms in the example of FIG. 2. The gate of the shunt FET is connected through a resistor 36 to a control signal line 38. As further discussed below, a control signal is applied through line 38 to the gate of shunt FET 34 to control conductance of FET 34, in response to variations of the attenuation control signal. Resistors 18, 36 provide RF isolation at the gates of FETs 20, 36, and have no other significant effect on operation of the attenuator circuit"

Barta et al discloses an arrangement in Fig. 2 a series FET 20 and a shunt FET 34 between as RF input/output terminals (22, 24) coupled along with respective capacitors and resistors(26, 28, 30, 32 and 36). This disclosed arrangement by Barta et al does not represent an electronic isolator. Barta et al at Figures 2, 6, 6a, 7 and 7a have the microwave connections labeled I/O (Input/Output), highlighting their interchangeability characteristics and symmetric attenuation regardless of the nature and state of the FETs (20 & 34). In providing test results (see Barta et al at Figures 4 and 5) for the preferred implementation, Barta et al gives a single result for each conduction, not separate values for forward and reverse measurements. Hence, Barta et al. anticipates symmetric characteristics and attenuation, which is unlike electronic isolators that have highly asymmetric attenuation of the electrical signal passing between source stage and load stage (see first paragraph of Summary in the present patent application). Therefore, Barta et al. does not teach, suggest or describe an electronic isolator let alone anticipate an electronic isolator between a source stage and a load stage.

CONCLUSION

For at least foregoing reasons, Applicant submits that the cited art does not teach or suggest, let alone anticipate, claims 1-4, 13, 14, 16, 21, 57, and 69 of the present application. In view of above, it is submitted that the claims now in the application, i.e., claims 1-4, 13, 14, 16, 21, 57, and 69 are in condition for allowance.

Respectfully submitted,

COUDERT BROTHERS LLP

Date: August 14, 2002 By: _____

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